



Operational Amplifiers/Buffers

LF351 Wide Bandwidth JFET Input Operational Amplifier

General Description

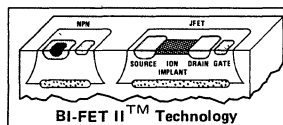
The LF351 is a low cost high speed JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF351 is pin compatible with the standard LM741 and uses the same offset voltage adjustment circuitry. This feature allows designers to immediately upgrade the overall performance of existing LM741 designs.

The LF351 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift, but for applica-

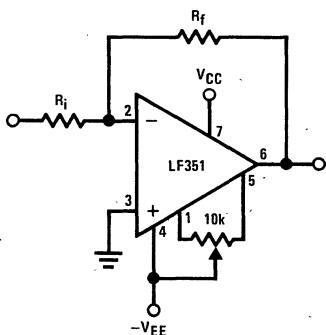
tions where these requirements are critical, the LF356 is recommended. If maximum supply current is important, however, the LF351 is the better choice.

Features

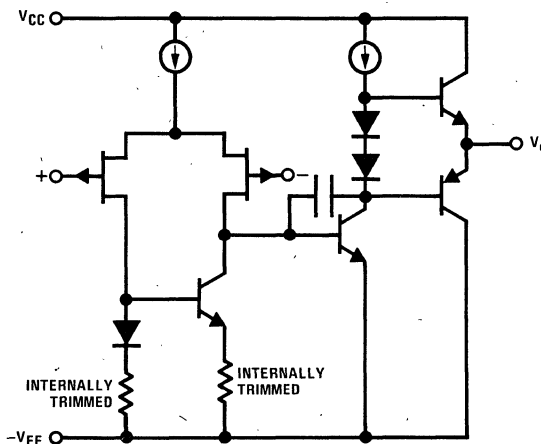
- Internally trimmed offset voltage 2 mV
- Low input bias current 50 pA
- Low input noise voltage 16 nV/√Hz
- Low input noise current 0.01 pA/√Hz
- Wide gain bandwidth 4 MHz
- High slew rate 13 V/μs
- Low supply current 1.8 mA
- High input impedance 1012Ω
- Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20$ Vp-p, BW = 20 Hz–20 kHz <0.02%
- Low 1/f noise corner 50 Hz
- Fast settling time to 0.01% 2 μs



Typical Connection

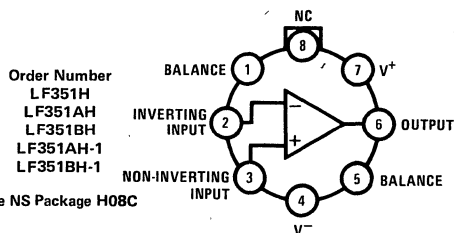


Simplified Schematic



Connection Diagrams (Top Views)

Metal Can Package

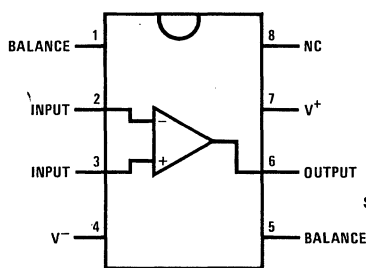


Order Number
LF351H
LF351AH
LF351BH
LF351AH-1
LF351BH-1

See NS Package H08C

Note. Pin 4 connected to case.

Dual-In-Line Package



Order Number
LF351N
LF351AN
LF351BN
LF351AN-1
LF351BN-1

See NS Package N08B

TOP VIEW

Absolute Maximum Ratings

Supply Voltage	±18V
Power Dissipation (Note 1)	500 mW
Operating Temperature Range	0°C to +70°C
T _j (MAX)	115°C
Differential Input Voltage	±30V
Input Voltage Range (Note 2)	±15V
Output Short Circuit Duration	Continuous
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LF351A			LF351B			LF351			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V _{OS}	Input Offset Voltage	R _S = 10 kΩ, T _A = 25°C Over Temperature		1	2 4		3	5 7		5	10 13	mV mV
ΔV _{OS} /ΔT	Average TC of Input Offset Voltage	R _S = 10 kΩ LF351A-1, LF351B-1		10			10			10		μV/°C
I _{OS}	Input Offset Current	T _j = 25°C, (Notes 3, 4) T _j ≤ 70°C		25	100 2		25	100 4		25	100 4	pA nA
I _B	Input Bias Current	T _j = 25°C, (Notes 3, 4) T _j ≤ 70°C		50	200 4		50	200 8		50	200 8	pA nA
R _{IN}	Input Resistance	T _j = 25°C		10 ¹²			10 ¹²			10 ¹²		Ω
A _{VOL}	Large Signal Voltage Gain	V _S = ±15V, T _A = 25°C V _O = ±10V, R _L = 2 kΩ Over Temperature	50	100		50	100		25	100		V/mV V/mV
V _O	Output Voltage Swing	V _S = ±15V, R _L = 10 kΩ	±12	±13.5		±12	±13.5		±12	±13.5		V
V _{CM}	Input Common-Mode Voltage Range	V _S = ±15V	±11	+15 -12		±11	+15 -12		±11	+15 -12		V V
CMRR	Common-Mode Rejection Ratio	R _S ≤ 10 kΩ	80	100		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 5)	80	100		80	100		70	100		dB
I _S	Supply Current			1.8	2.8		1.8	2.8		1.8	3.4	mA

AC Electrical Characteristics (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LF351A			LF351B			LF351			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew Rate	V _S = ±15V, T _A = 25°C	10	13			13			13		V/μs
GBW	Gain Bandwidth Product	V _S = ±15V, T _A = 25°C	3	4			4			4		MHz
e _n	Equivalent Input Noise Voltage	T _A = 25°C, R _S = 100Ω, f = 1000 Hz		16			16			16		nV/√Hz
i _n	Equivalent Input Noise Current	T _j = 25°C, f = 1000 Hz		0.01			0.01			0.01		pA/√Hz

Note 1: For operating at elevated temperature, the device must be derated based on a thermal resistance of 150°C/W junction to ambient or 45°C/W junction to case.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

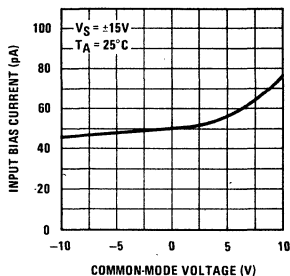
Note 3: These specifications apply for V_S = ±15V and 0°C ≤ T_A ≤ +70°C. V_{OS}, I_B and I_{OS} are measured at V_{CM} = 0.

Note 4: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. T_j = T_A + Θ_{JA} P_D where Θ_{JA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

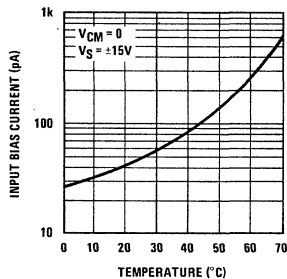
Note 5: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice.

Typical Performance Characteristics

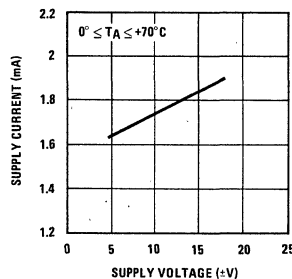
Input Bias Current



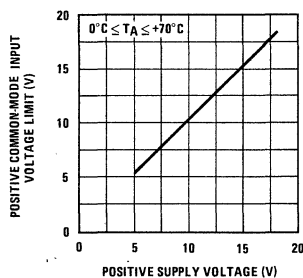
Input Bias Current



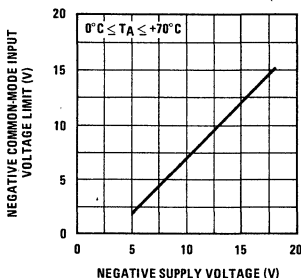
Supply Current



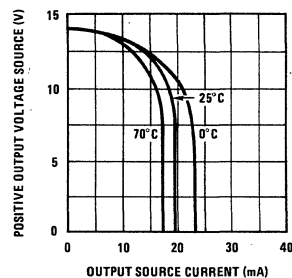
Positive Common-Mode Input Voltage Limit



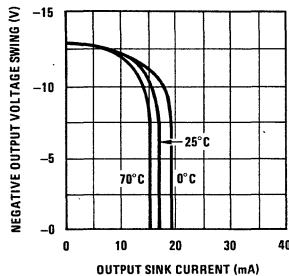
Negative Common-Mode Input Voltage Limit



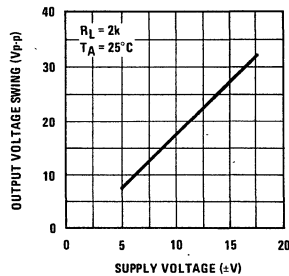
Positive Current Limit



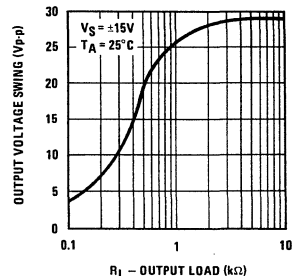
Negative Current Limit



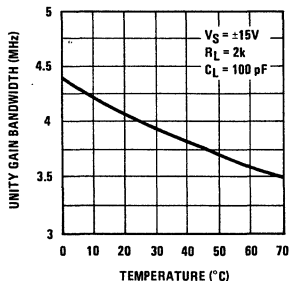
Voltage Swing



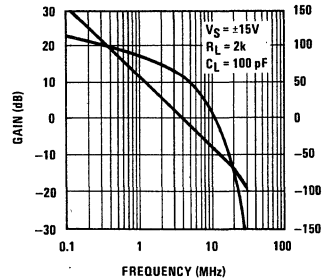
Output Voltage Swing



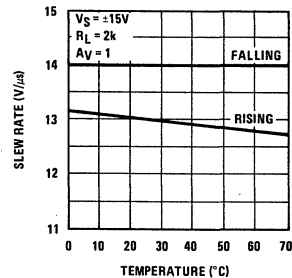
Gain Bandwidth



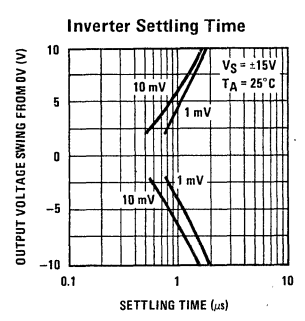
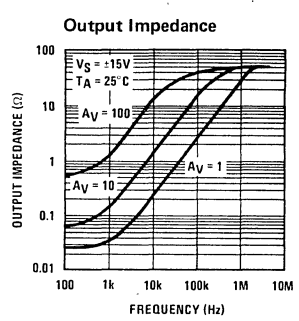
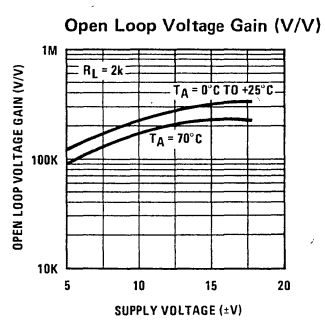
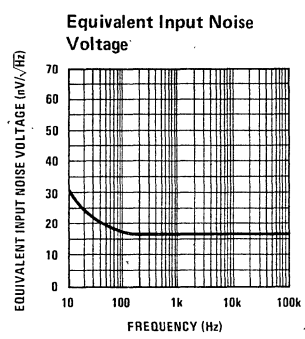
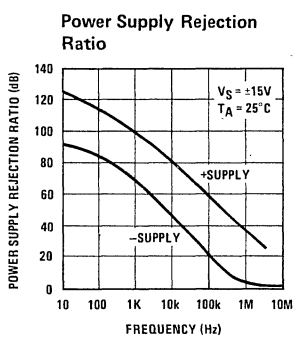
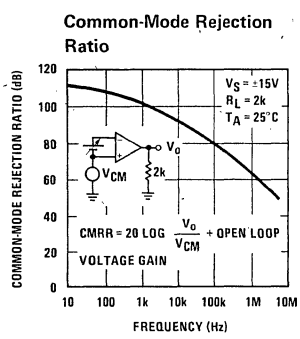
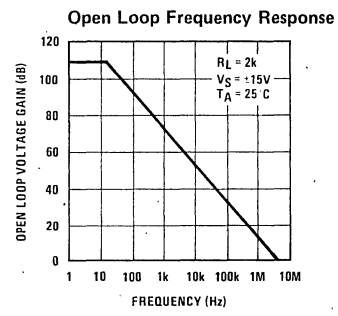
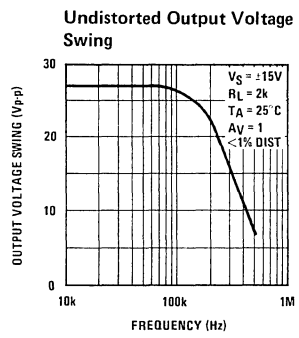
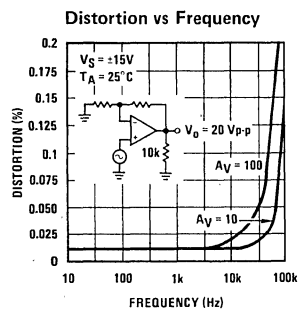
Bode Plot



Slew Rate

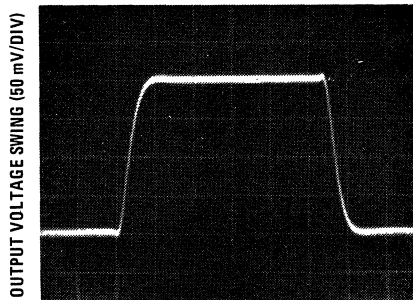


Typical Performance Characteristics (Continued)



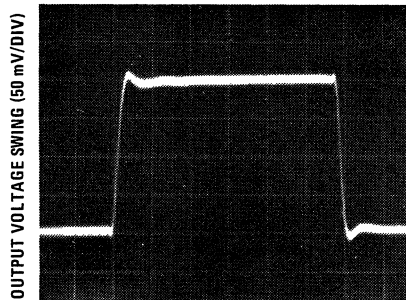
Pulse Response

Small Signal Inverting



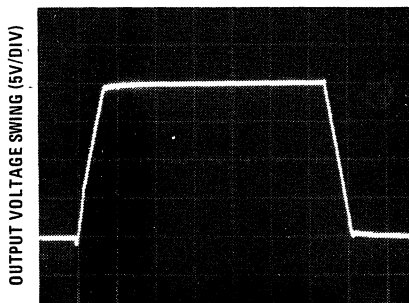
TIME (0.2 μ s/DIV)

Small Signal Non-Inverting



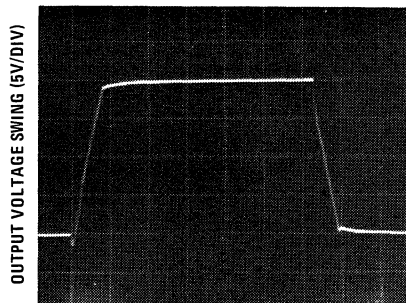
TIME (0.2 μ s/DIV)

Large Signal Inverting



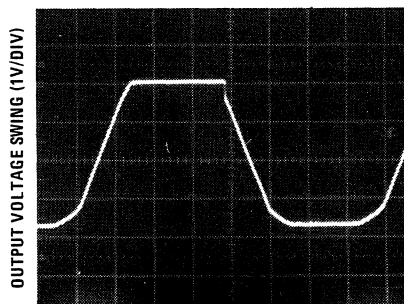
TIME (2 μ s/DIV)

Large Signal Non-Inverting



TIME (2 μ s/DIV)

Current Limit ($R_L = 100\Omega$)



TIME (5 μ s/DIV)

Application Hints

The LF351 is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II™). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be

allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a

Application Hints (Continued)

high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The LF351 is biased by a zener reference which allows normal circuit operation on $\pm 4V$ power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF351 will drive a $2\text{ k}\Omega$ load resistance to $\pm 10V$ over the full temperature range of 0°C to $+70^\circ\text{C}$. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed

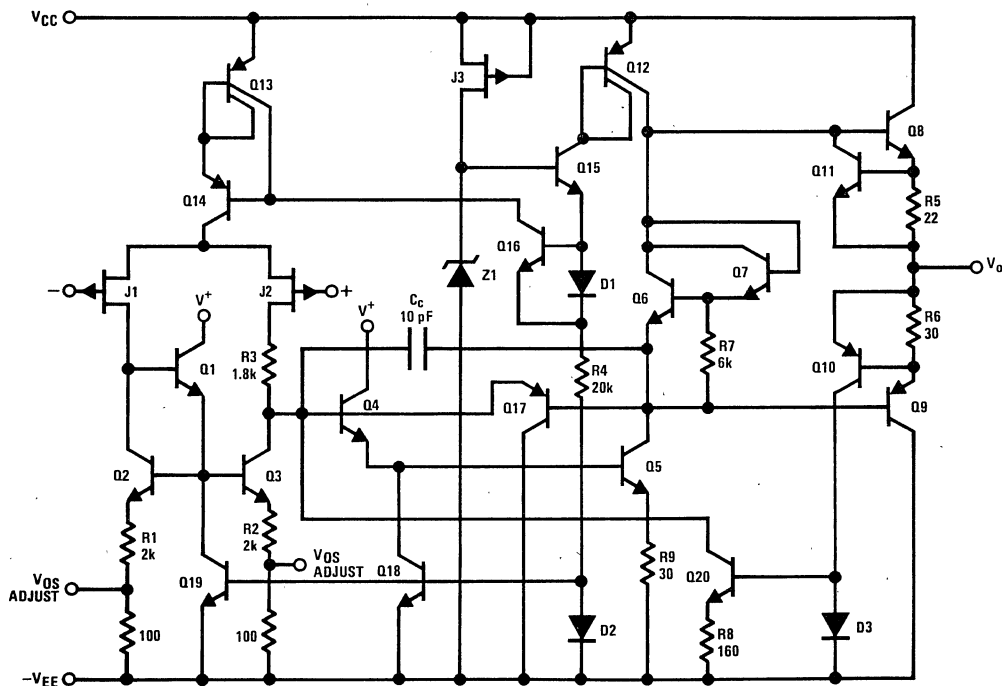
backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

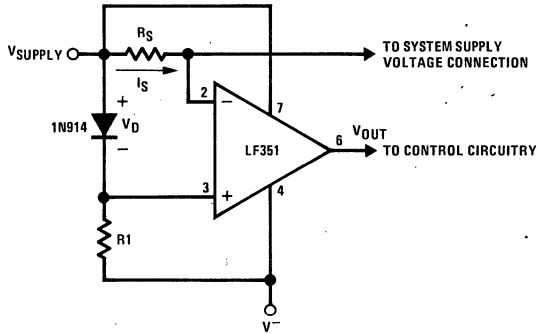
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Detailed Schematic



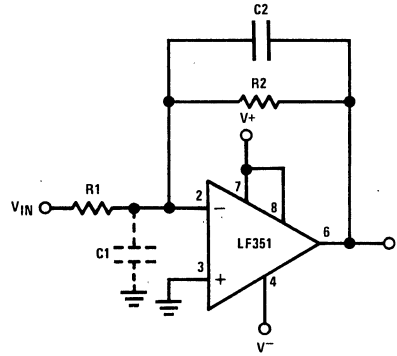
Typical Applications

Supply Current Indicator/Limiter



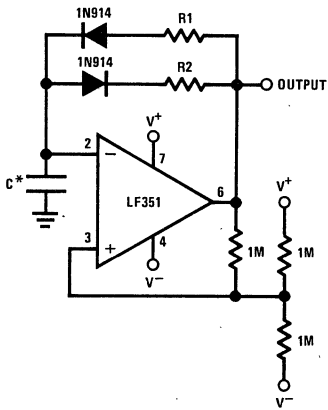
- V_{OUT} switches high when $R_S I_S > V_D$

Hi- Z_{IN} Inverting Amplifier



Parasitic input capacitance $C1 \approx (3 \text{ pF for LF351 plus any additional layout capacitance})$ interacts with feedback elements and creates undesirable high frequency pole. To compensate, add $C2$ such that: $R2C2 \approx R1C1$.

Ultra-Low (or High) Duty Cycle Pulse Generator

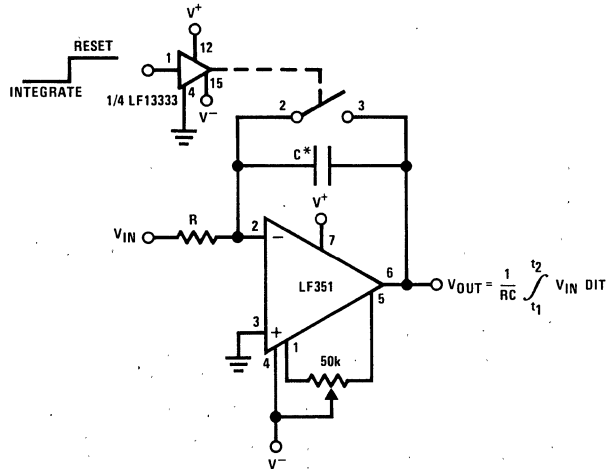


- $t_{OUTPUT \text{ HIGH}} \approx R1C \ln \frac{4.8 - 2V_S}{4.8 - V_S}$
- $t_{OUTPUT \text{ LOW}} \approx R2C \ln \frac{2V_S - 7.8}{V_S - 7.8}$

where $V_S = V^+ + |V^-|$

* low leakage capacitor

Long Time Integrator



* Low leakage capacitor

- 50k pot used for less sensitive V_{OS} adjust